ROBERT E. BUSHNELL*†

HENRY M. ZYKORIE
JOSEPH G. SEEBER°
JOHN C. BROSKY°+*
DARREN R. CREW+*
RUY M. GARCIA-ZAMOR*†

MICHAEL D. PARKER
DANIEL A. GESELOWITZ, PH.D.
(REG. PATENT AGENTS)

† ADMITTED IN MARYLAND
° ADMITTED IN VIRGINIA
+ ADMITTED IN PENNSYLVANIA
* NOT ADMITTED IN D.C.

R. E. BUSHNELL
ATTORNEY AT LAW
THE INVESTMENT BUILDING
1511 K STREET, N.W., SUITE 425
WASHINGTON, D.C. 20005-1401
UNITED STATES OF AMERICA

INTELLECTUAL PROPERTY LAW

TELEPHONE (202) 638-5740
(202) 638-2011
FACSIMILE (202) 628-0755
FACSIMILE (202) 628-3835
(410) 747-0022
E-MAIL: 2064566@MCIMAIL.COM

16 December 1998

❑ *U.S. Postal Service*
❑ *Via Local Courier*
❑ *Via International Courier*
❑ *Via Facsimile No.* _____
❑ *Via E-Mail Attachment*
❑ *Please Acknowledge Receipt*

Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Docket: P55281

Sir:

Submitted herewith is the following patent application:

Inventor: **SUNG-GON JUN**

Title: **FLAT PANEL DISPLAY AND DIGITAL DATA PROCESSING DEVICE USED THEREIN**

Please find attached hereto an application for patent which includes: Specification and Abstract, Claims, original Declaration And Power of Attorney, Assignment, and a certified copy of the foreign priority document identified below:

Verified Showing of Small Entity Status: **NO**

Drawings: Formal drawings, 2 sheets, Figures 1 through 2

Claim of priority under 35 U.S.C. §119: **YES**

** The Republic Of Korea Application No. 37478/1997 filed on 16 December 1997.

FEE (see formula below): **CHECK IS NOT ENCLOSED**

Basic Fee $380/760	$760.00
Additional Fees:	
Total number of claims in excess of 20__ times $9/18 .	$0.00
Number of independent claims in excess of 3: __ times $39/78	$0.00
Multiple Dependent Claims $130/260	$0.00
An Assignment is likewise enclosed: Recording Fee $40 . .	$0.00
Filing Non-English specification	$0.00
TOTAL FEES FOR THE ABOVE APPLICATION	***$760.00***

Docket No.: P55281

Inventor: **SUNG-GON JUN**

Title: **FLAT PANEL DISPLAY AND DIGITAL DATA PROCESSING DEVICE USED THEREIN**

In view of the above, it is requested that this application be accorded a filing date pursuant to 37 CFR 1.53(b).

Please address all correspondence to:

Robert E. Bushnell
1511 K Street, N.W.
Suite 425
Washington, D.C. 20005

Respectfully submitted,

Robert E. Bushnell
(Registration No. 27,774)
Payor No.: 008-439
Attorney for the Applicant
1522 K Street, N.W.
Suite 300
Washington, D.C. 20005

Telephone: (202) 638-5740
Telefacsimile: (202) 628-0755

REB/kf

TITLE

FLAT PANEL DISPLAY AND DIGITAL DATA PROCESSING DEVICE USED THEREIN

CLAIM OF PRIORITY

This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application for *FLAT PANEL DISPLAY AND DIGITAL DATA PROCESSING DEVICE USED THEREIN* earlier filed in the Korean Industrial Property Office on the 16th of December 1997 and there duly assigned Serial No. 37478/1997.

BACKGROUND OF THE INVENTION

Field of The Invention

The present invention concerns a flat panel display for receiving display information by means of a digital communication, and a digital processing device for utilizing it to connect to an analog display.

Description of the Related Art

It has been usual for a digital processing device such as a personal computer system to use a CRT (Cathode Ray Tube) for a display. Nowadays, a flat panel display such as an LCD (Liquid Crystal Display) or plasma display is also widely used. Such a flat panel display reproduces the image by converting the video signal received from a host such as a personal computer system to

corresponding digital data.

An LCD system generally includes an ADC (Analog-to-Digital Converter), a PLL circuit (Phase Locked Loop), a video data converter, an LCD driver, and an LCD panel the ADC converts an analog R(red), G(green) and B(blue) video signal to corresponding digital video data. The PLL circuit generates an internal clock signal in response to a synchronizing signal received from a host. The video data converter converts the digital video data according to a clock signal. This is to accommodate the dot and line numbers of the video data supplied to the LCD driver when the resolution provided by the host differs from that of the display. The LCD panel is driven by the LCD driver, displaying the video signal. Such a flat panel display system suffers from the following drawbacks:

The ADC for converting the analog video signal of the host to the digital video signal must perform the sampling operation at the rate of at least twice the frequency of the analog video signal. Additionally, the PLL circuit must have a wide locking range. This causes considerable increase of the overall production cost of the flat panel display. Moreover, a signal loss may frequently occur as well as jittering during analog-to-digital conversion, making the conversion unstable. Further, the allowable frequency range of the input signal is very limited owing to the operational characteristics of the ADC and PLL circuit. In addition, the screen size of the flat panel display is generally so small that it is inconvenient to make a presentation to many people.

The following each disclose features in common with the present invention: U.S. Patent No. 5,608,418 to McNally, entitled *Flat Panel Display Interface For A High Resolution Computer Graphics System*, U.S. Patent No. 5,491,496 to Tomiyasu, entitled *Display Control Device For Use*

With Flat-Panel Display And Color CRT Display, U.S. Patent No. 5,606,348 to Chiu, entitled *Programmable Display Interface Device And Method*, U.S. Patent No. 5,479,183 to Fujimoto, entitled *Apparatus And Method For Detecting An Optical CRT Display Connected To A Computer System*, U.S. Patent No. 5,828,349 to MacHesney *et al.*, entitled *Method And System For Multiplexing And Demultiplexing Video Signals For Graphic Display Monitors In Computer Systems*, U.S. Patent No. 5,841,418 to Bril *et al.*, entitled *Dual Displays Having Independent Resolutions And Refresh Rates*, U.S. Patent No. 5,764,201 to Ranganathan, entitled *Multiplexed Yuv-Movie Pixel Path For Driving Dual Displays*, U.S. Patent No. 5,710,570 to Wada *et al.*, entitled *Information Processing Unit Having Display Functions*, U.S. Patent No. 5,673,058 to Uragami *et al.*, entitled *One-Chip Semiconductor Integrated Circuit Device Capable Of Outputting Analog Color Signal Or Digital Color Signal*, U.S. Patent No. 5,629,715 to Zenda, entitled *Display Control System*, U.S. Patent No. 5.694.141 to Chee, entitled *Computer System With Double Simultaneous Displays Showing Differing Display Images*, U.S. Patent No. 5,579,025 to Itoh, entitled *Display Control Device For Controlling First And Second Displays Of Different Types*, and U.S. Patent No. 5,534,883 to Koh, entitled *Video Signal Interface.*

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a flat panel display which displays digital display information supplied by a digital data processing device.

It is another object of the present invention to provide a flat panel display with means for connecting to an analog display, which may make a convenient presentation to many people.

According to an embodiment of the present invention, a flat panel display for receiving display information including video data and synchronizing data from a host processing digital data in a serial digital communication, comprises: a receiver for reconstructing the display information, a synchronizing signal generator for generating a synchronizing signal by extracting the synchronizing data from the reconstructed display information, a digital-to-analog converter (DAC) for converting the video data to a corresponding video signal, and an output terminal for externally transferring the synchronizing signal and analog video signal to an analog display.

Preferably, a video data converter is further included to convert the line and dot numbers of the video data so as to correspond to a prescribed display mode when the synchronizing data has a different characteristic from the prescribed display mode. The synchronizing signal generator is accommodated to generate the synchronizing signal corresponding to the display mode.

According to another embodiment of the present invention, there is provided a digital data processing device, which may be used in a flat panel display for displaying display information received from a host processing digital data, and comprises: a transmitter connected to the host to transfer digital display information in serial data, a receiver for reconstructing the display information, a synchronizing signal generator for generating a synchronizing signal by extracting the synchronizing data from the reconstructed display information, a DAC for converting the video data to a corresponding video signal, and an output terminal for externally transferring the synchronizing signal and analog video signal to an analog display. The flat panel display includes the receiver, synchronizing signal generator and output terminal.

Preferably, a video data converter is further included to convert the line and dot numbers of

the video data so as to correspond to a prescribed display mode when the synchronizing data has a different characteristic from the prescribed display mode. The synchronizing signal generator is accommodated to generate the synchronizing signal corresponding to the display mode.

Thus, the host provides the display information as serial digital data, which is transferred to the flat panel display to display the digital video signal, and/or converted to an analog video signal, which is supplied to an analog display to display the analog video signal according to the synchronizing signal.

The present invention will now be described more specifically with reference to the drawings attached only by way of example.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

Fig. 1 is a block diagram for schematically showing the circuit of an earlier LCD system; and

Fig. 2 is a block diagram for schematically showing the circuit of an LCD system provided with means for connecting to a CRT according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram of the LCD system discussed in the Description of the Related Art

above.

The illustrated LCD system includes an ADC 210, a PLL circuit 220, a video data converter 230, an LCD driver 240, and an LCD panel 250. The ADC 210 converts an analog video signal 102 to corresponding to digital video data 212. The PLL circuit 220 generates an internal clock signal in response to a synchronizing signal 104 received from a host 100. The video data converter 230 converts the digital video data 212 according to a clock signal 222. This is to accommodate the dot and line numbers of the video data supplied to the LCD driver 240 when the resolution provided by the host 100 differs from that of the display. The LCD panel 250 is driven by the LCD driver 240 displaying the video signal.

Referring to Fig. 2, a host 300 is provided with a transmitter 310 to transfer display information 312 by means of a digital communication, for example, according to the IEEE 1394 format. The inventive LCD system 400 includes a receiver 410, a video data converter 420, a synchronizing signal generator 430, an LCD driver 240, a RAMDAC 440, an output terminal 450, and an LCD panel 250.

The receiver 410 reconstructs the display information 312 received from the transmitter 310 to provide the video data converter 420 with data 412 including R, G, B video data and a dot clock signal. The video data converter 420, if a conversion of the video data is required, changes the dot and line numbers of the video data to correspond to the resolution supported by the LCD 400, delivering the converted video data 422 to the LCD driver 240. On the other hand, the converted video data 414 is supplied to the RAMDAC 440 to convert to the analog R, G, B video signal 442 delivered to the output terminal 450. Synchronizing data 414 for horizontal and vertical

synchronization is supplied to the synchronizing signal generator 430 to generate a synchronizing signal 432 delivered to the output terminal for the analog display.

The analog display connected to the output terminal 450 may be, for example, a CRT display 500, which comprises an amplifier 510, a deflection signal generator 520, a high voltage generator 530, and a CRT 540. The CRT display 500 receives the analog video signal 442 and synchronizing signal 432 through the output terminal 450. The analog video signal 442 is amplified through the amplifier 510, which supplies the amplified video signal 512 to the CRT 540. The synchronizing signal 432 is transferred to the deflection signal generator 520 to supply the corresponding deflection signal 522 to the CRT 540.

Thus, the host 300 supplies serially the digital display data to the LCD 400 to display the image on the LCD panel 250 while the CRT display 500 connected to the output terminal 450 of the LCD 400 receives the analog video signal and synchronizing signal to display the image through the CRT 540.

As described above, the inventive flat panel display does not require a separate ADC because it receives the display information in digital data, and provides means for connecting an analog display.

It should be understood that the present invention is not limited to the particular embodiment disclosed herein as the best mode contemplated for carrying out the present invention, but rather that the present invention is not limited to the specific embodiments described in this specification except as defined in the appended claims.

WHAT IS CLAIMED IS:

1. A flat panel display for receiving display information including video data and synchronizing data from a host processing digital data in a serial digital communication, comprising:

a receiver for reconstructing said display information;

a synchronizing signal generator for generating a synchronizing signal by extracting the synchronizing data from said reconstructed display information;

a digital-to-analog converter (DAC) for converting said video data to a corresponding video signal; and

an output terminal for externally transferring said synchronizing signal and analog video signal to an analog display.

2. A flat panel display as defined in claim 1, further comprising a video data converter for converting line and dot numbers of said video data so as to correspond to a prescribed display mode when said synchronizing data has a different characteristic from said prescribed display mode, and said synchronizing signal generator generates said synchronizing signal corresponding to said display mode.

3. A digital data processing device used in a flat panel display for displaying display information received from a host processing digital data, comprising:

a transmitter connected to said host to transfer digital display information as serial data;

a receiver for reconstructing said display information;

a synchronizing signal generator for generating a synchronizing signal by extracting synchronizing data from said reconstructed display information;

a digital-to-analog converter (DAC) for converting video data to a corresponding video signal; and

an output terminal for externally transferring said synchronizing signal and analog video signal to an analog display, said flat panel display including said receiver, synchronizing signal generator and output terminal.

4. A flat panel display as defined in claim 2, further comprising a liquid crystal display (LCD) driver for receiving data output from said video data converter; and

a liquid crystal display (LCD) display panel for receiving an output from said LCD driver.

5. A flat panel display as defined in claim 1, said analog display comprising an amplifier for receiving said video signal from said DAC via said output terminal and amplifying said video signal;

a deflection signal generator for receiving said synchronizing signal output from aid synchronizing signal generator via said output terminal and for generating deflection signals;

a high voltage generator for receiving an output from said deflection signal generator and generating a high voltage;

a cathode ray tube (CRT) display for receiving said amplified video signal from said amplifier and output signals from said deflection signal generator and a high voltage from said high

voltage generator.

6. A digital data processing device used in a flat panel display as defined in claim 3, further comprising a video data converter for converting line and dot numbers of said video data so as to correspond to a prescribed display mode when said synchronizing data has a different characteristic from said prescribed display mode, and said synchronizing signal generator generates said synchronizing signal corresponding to said display mode.

7. A digital data processing device used in a flat panel display as defined in claim 6, further comprising a liquid crystal display (LCD) driver for receiving data output from said video data converter; and

a liquid crystal display (LCD) display panel for receiving an output from said LCD driver.

8. A digital data processing device used in a flat panel display as defined in claim 3, said analog display comprising an amplifier for receiving said video signal from said DAC via said output terminal and amplifying said video signal;

a deflection signal generator for receiving said synchronizing signal output from aid synchronizing signal generator via said output terminal and for generating deflection signals;

a high voltage generator for receiving an output from said deflection signal generator and generating a high voltage;

a cathode ray tube (CRT) display for receiving said amplified video signal from said

amplifier and output signals from said deflection signal generator and a high voltage from said high voltage generator.

ABSTRACT

A flat panel display for receiving digital display information including video data and synchronizing data from a host includes: a receiver for reconstructing the display information, a synchronizing signal generator for generating a synchronizing signal by extracting the synchronizing data from the reconstructed display information, a digital-to-analog converter for converting the video data to a corresponding video signal, and an output terminal for externally transferring the synchronizing signal and analog video signal to an analog display. A video data converter is further included to convert line and dot numbers of the video data so as to correspond to a prescribed display mode when the synchronizing data has a different characteristic from the prescribed display mode. The synchronizing signal generator generates the synchronizing signal corresponding to the display mode.

PATENT
P55281

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

SUNG-GON JUN

Serial No.:	*to be assigned*	Examiner:	*to be assigned*
Filed:	16 December 1998	Art Unit:	*to be assigned*

For: FLAT PANEL DISPLAY AND DIGITAL DATA PROCESSING DEVICE USED THEREIN

TRANSMITTAL OF DECLARATION

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

This transmittal accompanies a Declaration without the signature by the inventor(s), for the above-captioned application. A Substitute Declaration with the inventor(s)'s signature will be filed upon receipt of the Serial No. for the above-captioned application.

Respectfully submitted,

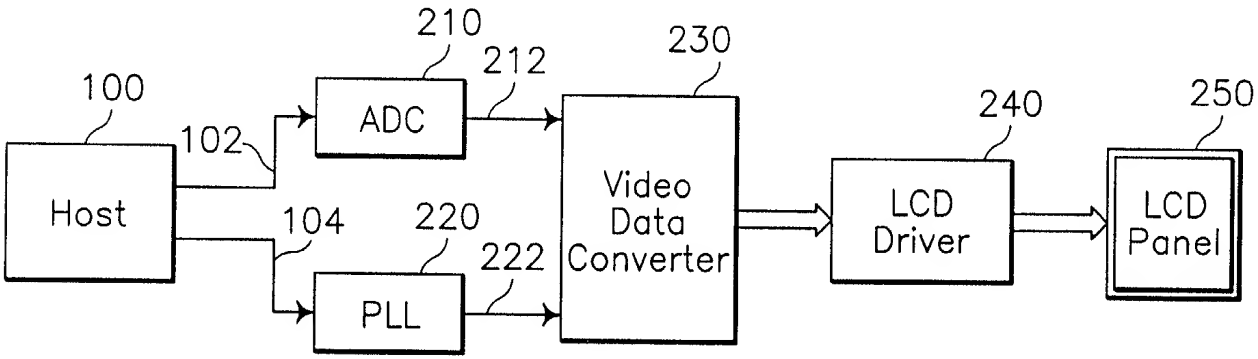
Robert E. Bushnell,
Attorney for the Applicant
Registration No.: 27,774

Suite 300, 1522 "K" Street, N.W.
Washington, D.C. 20005
(202) 638-5740

Folio: P55281
Date: 12/16/98
I.D.: REB/kf

Fig. 1

(Related Art)



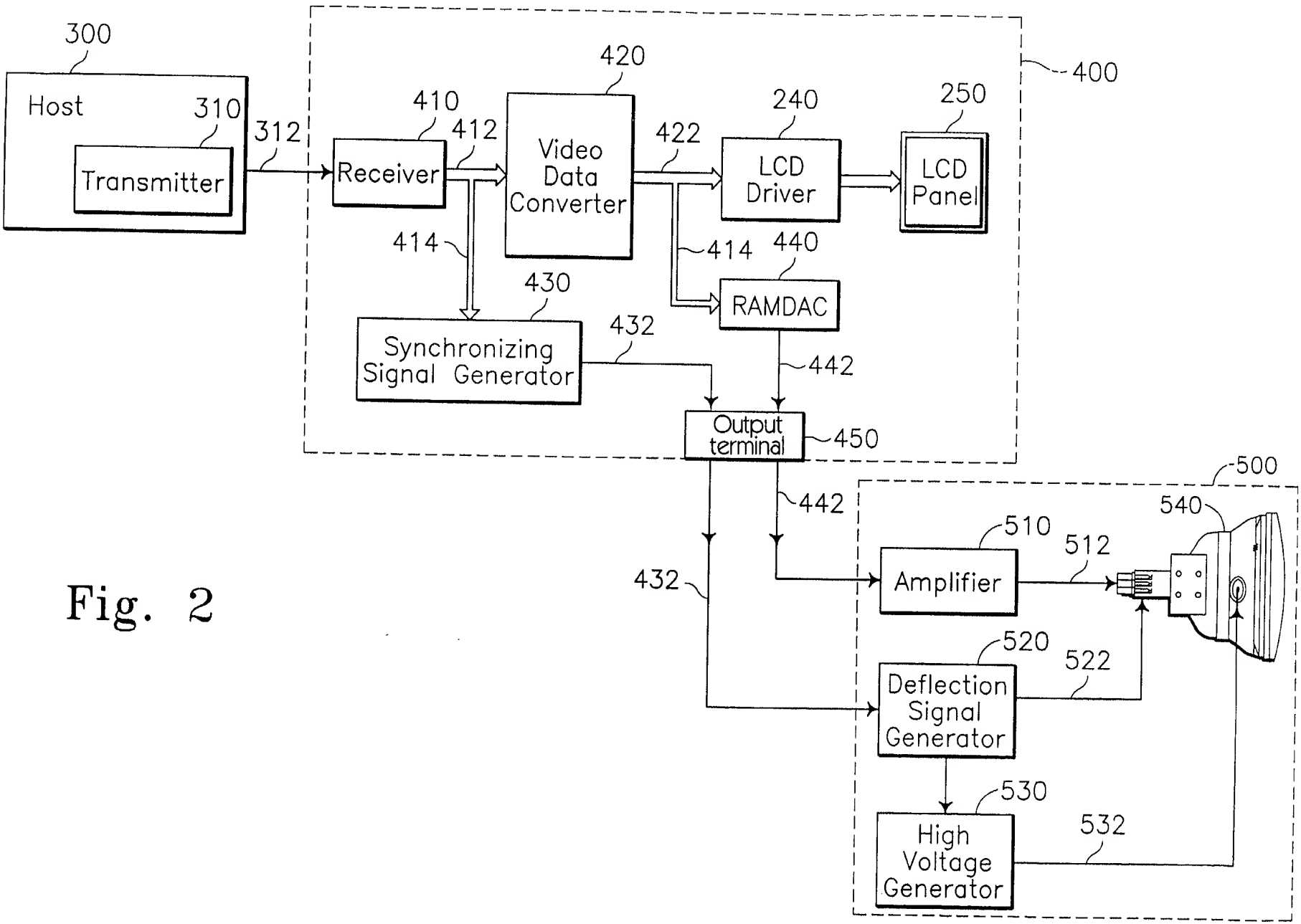

300
Host
310
Transmitter
312
400
420
410
412
Receiver
Video
Data
Converter
422
240
LCD
Driver
250
LCD
Panel
414
414
440
RAMDAC
430
Synchronizing
Signal Generator
432
442
Output
terminal
450
500
442
540
510
512
Amplifier
432
520
522
Deflection
Signal
Generator
530
532
High
Voltage
Generator

Fig. 2

PTO/SB/01 (6/95)

DECLARATION

Docket No. P55281

AS A BELOW NAMED INVENTOR, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole (*if only one name is listed below*), or an original, first and joint inventor (*if plural names are listed below*), of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: *FLAT PANEL DISPLAY AND DIGITAL DATA PROCESSING DEVICE USED THEREIN*

the specification of which either is attached hereto or otherwise accompanies this Declaration, or:

☐ was filed in the U.S. Patent & Trademark Office on _____ and assigned Serial No._____,

☐ and (*if applicable*) was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations §1.56. I hereby claim foreign priority benefits under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

			Priority Claimed:
37478/1997	Republic of Korea	16 December 1997	Yes [X] No [ ]
(Application Number)	*(Country)*	*(Day/Month/Year filed)*	
			Yes [ ] No [ ]
(Application Number)	*(Country)*	*(Day/Month/Year filed)*	

I hereby claim the benefit under Title 35, U.S. Code, §120, of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	*(Filing Date)*	*(STATUS: patented, pending, abandoned)*
(Application Serial No.)	*(Filing Date)*	*(STATUS: patented, pending, abandoned)*

I hereby revoke all previously granted powers of attorney and appoint the following attorneys: Robert E. Bushnell, Reg. No. 27,774, Michael D. Parker, Reg. No. 34,973, and Henry M. Zykorie, Reg. No. 27,477, to prosecute this application and to transact all business in the U.S. Patent & Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

Robert E. Bushnell,
Attorney-at-Law
Suite 300, 1522 "K" Street, N.W.
Washington, D.C. 20005-1202

Payor No. 008439
Area Code: 202-638-5740

I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST OR SOLE INVENTOR: SUNG-GON JUN Citizenship: Republic of Korea

Inventor's signature: _____ Date: _____

Residence & Post Office Address: 1012-16 Ingea-dong, Paldal-ku, Suwon, Kyunggi-do, Republic of Korea

FULL NAME OF SECOND JOINT INVENTOR: _____ Citizenship: _____

Inventor's signature: _____ Date: _____

Residence & Post Office Address:

FULL NAME OF THIRD JOINT INVENTOR: _____ Citizenship: _____

Inventor's signature: _____ Date: _____

Residence & Post Office Address:

FULL NAME OF FOURTH JOINT INVENTOR: _____ Citizenship: _____

Inventor's signature: _____ Date: _____

Residence & Post Office Address: